Inter Integrated Circuit (I2C)

I2C Features (1/2)

- Multi Master and slave capability
- Controls all I²C bus specific sequencing, protocol, arbitration and timing
- Standard and fast I²C mode (up to 400kHz)
- 7-bit and 10-bit addressing modes
- Status flags:
  - Transmitter/Receiver mode flag
  - End-of-Byte transmission flag
  - I2C busy flag

New on 15x devices

- Configurable PEC (Packet Error Checking) Generation or Verification:
  - based on CRC-8 ($x^8 + x^2 + x + 1$)
  - PEC value can be transmitted as last byte in Tx mode
  - PEC error checking for last received byte / dedicated interrupt

I2C Features (2/2)

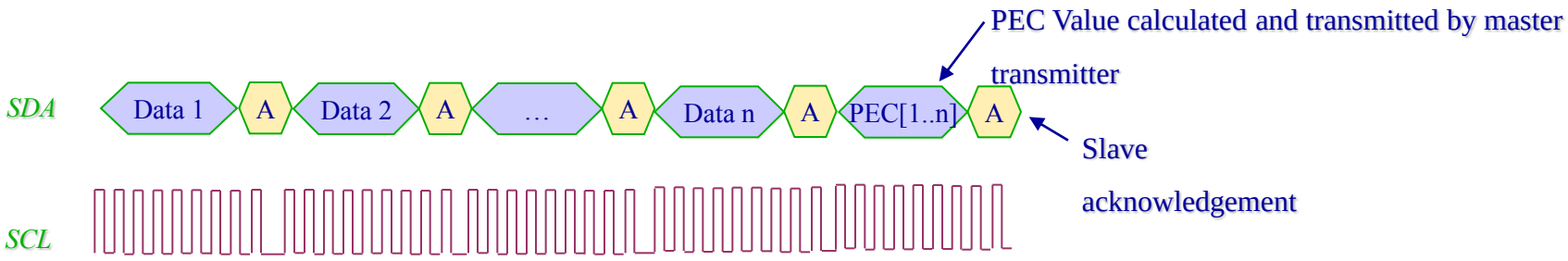
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/ data transmission
  - Detection of misplaced start or stop condition
  - Overrun/Underrun if clock stretching is disabled
- 2 Interrupt vectors:
  - 1 Interrupt for successful address/ data communication
  - 1 Interrupt for error condition
- 1-byte buffer with DMA capability
- SMBus 2.0 Compatibility
- PMBus Compatibility

DMA Capability

- The I2C has a DMA Tx and Rx requests
- The I2C requests is mapped on a different DMA channel: possibility to use DMA for both I2C transfer direction in the same time
- Calculated PEC value is automatically transmitted at the end of data transfer

PEC

- Example of a n data transfer between a master transmitter and a slave receiver followed by the PEC transmission



SMBus Mode

- SMBus 2.0 Compatibility
- Low cost and more robust than I²C
- Clock synchronization mechanism allow devices of different speeds to co-exist on the bus:
  - Clock low extending:
    - 10ms master cumulative clock low extend time
    - 25ms slave cumulative clock low extend time
  - Clock stretching on every bit transfer
- Timeout: 25ms clock low timeout delay
- Hardware Packet Error Checking (PEC) generation/verification with ACK control
- Address Resolution Protocol (ARP) supported
- SMBALERT# line for interrupts
- Host Notify Protocol

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